California State University, Fullerton

Computer Engineering

**EGCP 446 – Advanced Digital Design using Verilog HDL**

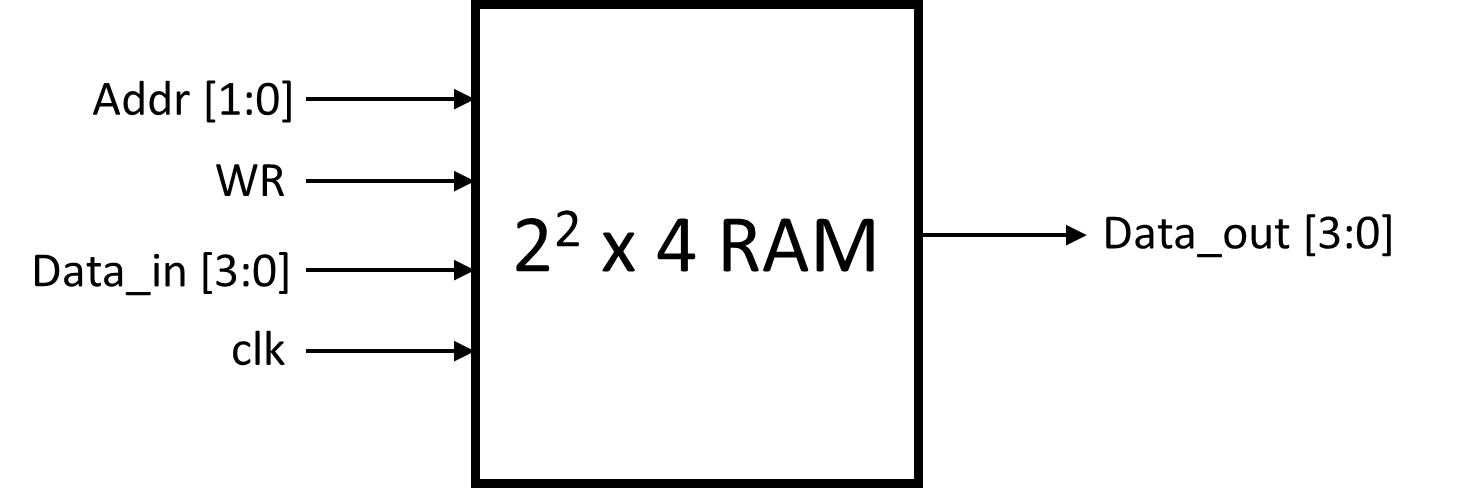
**(Fall 2019)**

**Lab No 4: RAM**

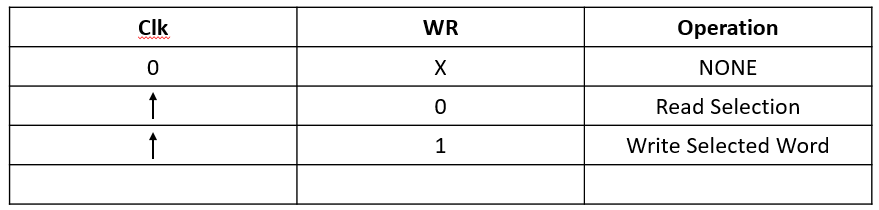
1. **Lab Description**

**Part A: Clock Divider**

Implement following 4-bit with each cell with 4-bit long.



**Table I RAM operation description**



Use the Verilog code provided with the lab to implement it on FPGA board. Connect clk with the system clock, WR with the swtich, Addr and Data\_in with the swtiches, and Data\_out with the LED.

***Stores input if W = 1 into wordline specified by ADDR, reads wordline if W = 0***

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Submit your Verilog, Picture of FPGA, ASM diagram and UCF file

Verilog Code:

module RAM(addr,clk,din,dout,we);

input [1:0] addr;

input clk;

input [3:0] din;

output [3:0] dout;

input we;

reg [3:0] Mem\_out[0:3];

always@(posedge clk)

begin

if(we)

Mem\_out[addr] <= din;

else

Mem\_out[addr] <= Mem\_out[addr];

end

assign dout = Mem\_out[addr];

endmodule

UCF:

# Clock

Net "clk" LOC = "T9";

NET "clk" PERIOD = 20ns; # 20ns = 50Mhz

#Net "Socket" LOC = "D9";

#NET "Socket" PERIOD = ??????? ns;

# User Switches

NET "din<0>" LOC = "F12";

NET "din<1>" LOC = "G12";

NET "din<2>" LOC = "H14";

NET "din<3>" LOC = "H13";

NET "addr<0>" LOC = "J14";

NET "addr<1>" LOC = "J13";

NET "we" LOC = "K14";

#NET "SW7" LOC = "K13";

# User Buttons

#NET "BTN0" LOC = "M13";

#NET "BTN1" LOC = "M14";

#NET "BTN2" LOC = "L13";

#NET "BTN3" LOC = "L14";

# LEDs

NET "dout<0>" LOC = "K12";

NET "dout<1>" LOC = "P14";

NET "dout<2>" LOC = "L12";

NET "dout<3>" LOC = "N14";

#NET "LD4" LOC = "P13";

#NET "LD5" LOC = "N12";

#NET "LD6" LOC = "P12";

#NET "LD7" LOC = "P11";

ASM Diagram:

Mem\_out[addr] <= Mem\_out[addr]

0

Mem\_out[addr] <= din

1

0

Posedge clk

we

1

Reset

assign Dout = Mem\_out[addr]

Pictures

